CLAIMS

1. A method of automatically performing a wafer simulation, the method comprising:

receiving a mask image;

performing a wafer simulation of the mask image using an optical model;

characterizing a feature from the mask image;

obtaining threshold data from a look-up table (LUT) based on characterizing, the LUT generated using a resist model; and

applying the threshold data to the wafer simulation to generate accurate wafer contours of the feature.

2. The method of Claim 1, wherein characterizing can include classifying the feature using at least one of pattern, feature size, and pitch.

3. The method of Claim 1, wherein obtaining threshold data can indicate an exact match or a closest match in the LUT.

4. A method of automatically performing a wafer simulation, the method comprising:

receiving a mask image;

performing a wafer simulation of the mask image using a first model;

characterizing a feature from the mask image;

obtaining threshold data from a look-up table (LUT) based on characterizing, the LUT generated using a second model more accurate than the first model; and

applying the threshold data to the wafer simulation to generate wafer contours of the feature.

5. The method of Claim 4, wherein characterizing can include classifying the feature using at least one of pattern, feature size, and pitch.

6. The method of Claim 4, wherein obtaining threshold data can indicate an exact match or a closest match in the LUT.

7. A method of determining a wafer contour of a mask feature, the method comprising:

simulating the wafer contour by applying an optical model to the mask feature;

accessing resist information to determine a threshold associated with the mask feature; and

improving an accuracy of the wafer contour using the threshold.

8. The method of Claim 7, wherein accessing the resist information includes accessing a look-up table (LUT) of a plurality of mask features and associated thresholds.

9. The method of Claim 8, wherein the LUT is organized based on at least one of pattern, feature size, and pitch size.

10. The method of Claim 7, wherein the resist information includes optical and resist information.

11. The method of Claim 7, wherein the resist information includes etch information in addition to resist information.

12. A computer-implemented program for generating a wafer contour, the program comprising:

code for receiving a mask image;

code for performing a wafer simulation of the mask image using an optical model;

code for characterizing a feature from the mask image;

code for obtaining threshold data from a look-up table (LUT) based on characterizing, the LUT generated using a resist model; and

code for applying the threshold data to the wafer simulation to generate accurate wafer contours of the feature.

13. The program of Claim 12, wherein code for characterizing can include code for classifying the feature using at least one of pattern, feature size, and pitch size.

14. The program of Claim 12, wherein code for obtaining threshold data can provide at least one of an exact match in the LUT and a closest match in the LUT.

15. A method of creating a look-up table (LUT) for use in a wafer simulation, the method including:

receiving a test layout;

simulating the test layout using a resist model, which provides accurate wafer edge locations of features on the test layout;

simulating the test layout using an optical model, which provides aerial image information of features on the test layout;

matching the wafer edge locations to the aerial image information;

computing thresholds for a plurality of features based on matching; and

storing the thresholds in the LUT.

16. The method of Claim 15, wherein thresholds vary for different patterns, pitch sizes, feature sizes, and defect types.

17. The method of Claim 15, wherein the LUT includes threshold and at least one of pattern, pitch size, feature size, and defect type.

18. The method of Claim 15, wherein the LUT can include the thresholds for more than one resist.

19. The method of Claim 15, wherein the aerial image information indicates light intensity as a function of position.

20. The method of Claim 15, wherein the test layout includes various patterns, pitch sizes, and feature sizes.

21. A look-up table (LUT) for use in a wafer simulation, the LUT including:

a plurality of mask features; and

a plurality of thresholds, wherein each mask feature has an associated threshold.